Low Voltage Polymer Transistors

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***Abstract*— The combination of polymer semiconducting 'inks' and relatively high resolution printing processes promises to make integrated printed circuits commercially viable. These circuits can be flexible and capital costs of production are very low. One of the key challenges to implementation of this technology is that most transistors made using polymer semiconductors have high operating voltages, which is not ideal for low power, low cost, battery compatible technology. We report on an organic metal semiconductor field effect transistor which operates at 3.5 V. In the initial implementation of this transistor poly(3-hexylthiophene) is the semiconductor, with an aluminium layer used as the gate electrode. The on/off current ratio of this device is only 24.6, but simulations suggest that an improvement of up to three orders of magnitude is possible. The fabrication process requires one less step than other organic transistors. It also uses the gate to encapsulate the transistor, limiting exposure oxygen and moisture, which are known to degrade their performance.**

Keywords- Organic Field Effect Transistor (OFET), Metal-Semiconductor Field Effect Transistor (MESFET), regioregular poly(3-hexylthiophene) (rr-P3HT), Schottky junction.

I. INTRODUCTION

Organic semiconductors hold the promise of revolutionizing certain aspects of the microelectronics industry. Chemists can tune certain properties of these compounds such as their bandgaps and reactivities, making them ideal for applications such as chemical sensors and color displays. These materials can be processed at room temperature, allowing their use with flexible transparent plastic substrates; something impossible for a-Si:H technology which requires temperatures as high as 360°C [1]. The most enticing aspect of these compounds is that some of them can be dissolved in organic solvents to make semiconducting 'inks'. These inks can then be processed into thin films with very inexpensive methods such as spin coating and inkjet printing.

There has been a significant effort made to build a reliable and practical organic thin film transistor (OTFT) with an insulated gate. Although these devices exhibit an on/off current ratio of about 10^6 [2], they require a high operating voltage to achieve this which reduces their attractiveness for use in portable devices. There are basically two ways of addressing this issue. One way is to deposit a more crystalline semiconductor layer. The other way is to increase the capacitance of the gate insulator, either by decreasing its thickness or using a material with a high dielectric constant. Unfortunately, these approaches are so far incompatible with inexpensive printing methods.

We propose a novel solution to this challenge which requires neither exotic materials nor expensive processing methods. We have designed and constructed an organic metal-semiconductor field effect transistor (OMESFET), which can be operated in the range of 5V and is less complicated to manufacture than an OTFT. The device is based on poly(3-hexylthiophene) (rr-P3HT), an intrinsically p-type conducting polymer with a high field effect mobility [3]. Section II discusses The OMESFET geometry, principles of operation, and simulated behavior. The construction and testing of a prototype is presented in section III. A discussion follows in section IV.

II. OMESFET PRINCIPLES

A. Device Geometry and Operation

The OMESFET geometry is depicted in figure 1. The geometry offers a couple of advantages over OTFTs. First, the absence of a gate insulator can simplify the manufacturing process by eliminating a step. Second, many organic semiconductors are sensitive to environmental oxygen and moisture which act as dopants[4]. By completely encapsulating the device, the gate protects it from this effect.

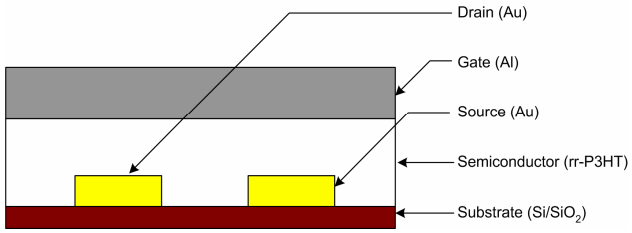

Fig. 1. OMESFET structure. Horizontal dimensions are not to scale.

As in any MESFET, the gate directly contacts the channel to form a Schottky junction. In this case, it is formed between the aluminum gate and the rr-P3HT channel. Aluminum was selected due to its low work function (4.2 eV [5]). The drain and source contacts are comprised of gold (work function of 5.4 eV[5]) in order to form ohmic contacts with the channel [6].

The difference between the work functions of the aluminum gate and the rr-P3HT channel sweeps mobile charge away from a region inside the channel that is immediately adjacent to the gate. This region of greatly reduced mobile charge, known as the depletion region, is insulating and has the effect of reducing the cross section of the channel. By driving the Schottky junction into reverse bias, the depth of the depletion region is increased. This allows control of the resistance between the source and drain. If the threshold voltage (V_T) is applied to the gate, the depletion region is extended to the entire depth of the channel and the OMESFET is turned off.

An analytical model of the device requires a precise knowledge of the depth of the depletion region as a function of applied voltage. This is easily done for the case of a MESFET based on a crystalline semiconductor such as Si or GaAs. This is possible because the immobile charge in the depletion region can be assumed to be due to ionized dopants. Since the doping distribution is known, so is the charge distribution, allowing the use of Poisson's equation to solve the depletion depth as a function of applied voltage. The case of a conducting polymer is much more complicated since the immobile charge is due to a large number of traps. An analytical expression would have to be derived from the density of states. A simpler approach to predicting the device's performance is to numerically model it.

B. Device Simulation

The simulation was done using the Medici 4.0 two-dimensional device simulator by Synopsis [7]. This software package solves the potential and charge carrier distributions in a two dimensional plane of the user defined device, treating the third dimension as normalized to 1 μm.

Since rr-P3HT is a p-type material the simulation only took holes into account. The semiconductor was simulated with localized states chosen so as to imitate the material's measured density of states [8].

The simulated device had the following dimensions. The channel as well as the drain and source contacts had a length of 4 μm. The semiconductor had a thickness of 400 nm, a value considered reasonable for an inkjet printer [9].

The simulation results indicated that the OMESFET could operate in both a linear and a saturation regime. The OMESFET showed a conductance of 1×10^{-13} S when fully on (V_{GS}=0 V). A transconductance of 2×10^{-14} S and a subthreshold swing of 180 mV/dec were found by varying V_{GS} while applying a constant small V_{DS}. The on/off current ratio was found to be 10^4 with a threshold voltage of 5 V.

The simulation indicated that for V_{DS} exceeding -10V the leakage current from the gate was of the same order of magnitude as the transistor's off current.

III. EXPERIMENTS

A. Manufacturing Process

In order to simplify manufacturing, and to have controlled conditions in the initial demonstration devices, the OMESFETs were built on an extremely flat and rigid substrate. Si wafers meet this requirement and have the added advantage of being widely available. Wafers from Silicon Quest International, Inc. [10] with a thermally grown oxide layer of 350 nm were used.

The gold electrodes were patterned with a photolithographic mask and deposited with an electron-beam evaporator to a thickness of 70 nm. Each electrode measured 500 μm by 4 μm with an inter-electrode distance of 4 μm.

Because rr-P3HT is oxygen and moisture sensitive, the electrodes were transferred to a glovebox where all subsequent steps were carried out under a N_2 environment. The glovebox used had been custom fitted with a thermal evaporator.

rr-P3HT was acquired from American Dye Source, Inc. [11] as a granular solid. It was dissolved in chloroform to form a 0.54 w.t. % solution which was used as a semiconducting 'ink'. A spin coater was initially used to deposit the 120 nm thick semiconductor films, but the results were not satisfactory as many attempts resulted in an ohmic path between the gate and the other two electrodes likely due to pinholes in the film. A thicker film reduces the chances of pinholes forming, but is difficult to achieve with spin coating. The film's thickness is increased if it is spun at a slower speed, this however makes a less regular film. An acceptable film was instead formed by dip casting. This simple process involves dipping the electrodes in the solution, and then slowly drawing them out, letting the solvent evaporate to leave a uniform film behind. A 200 nm thick film was deposited this way. Once the film was formed, the electrodes were baked on a hot plate at 120°C for 20 minutes so as to draw out any remaining chloroform.

The final step was the deposition of the aluminum gate. As noted above, the glovebox used contained a thermal evaporator so that this step could be done without exposing the sample to atmosphere. A shadow mask was used to pattern a gate 120 nm thick.

B. Measurement Techniques

All measurements of the OMESFET were done inside the glovebox. A Keithley 6430 SourceMeter was used to drive the gate and measure the leakage current. The drain to source voltage was driven by a Keithley 2400 SourceMeter which also measured the drain current.

C. Results

The performances of the real and simulated OMESFETs are compared in table 1.

TABLE I. PERFORMANCE COMPARISON

Metric	OMESFET, experimental	OMESFET, simulation
I_{ON}/I_{OFF}	24.6	10^4
V_T (V)	3.5	5
g_0 (S)	6.6×10^{-12}	1×10^{-13}
g_m (S)	2×10^{-11}	2×10^{-14}

g_0 and g_m values are normalized to a 1 μm channel width.

IV. DISCUSSION

Since several quantities were not well known at simulation time, a best case approach was taken which led to idealized performance predictions. The simulation results are nonetheless still valid both as a proof of concept and as an indication of the performance gains which may be possible.

The simulation correctly predicted a threshold voltage below 10 V. The measured value was actually lower than predicted; this was likely due to the semiconductor layer thickness being half the value used in simulation. This thinner layer meant there was less material to deplete in order to turn the device off.

The conductance and especially the transconductance of the device were larger than predicted. This is attributable to a larger carrier concentration than assumed in the simulation. This would indicate a significant doping level possibly due to contamination.

There is a difference of three orders of magnitude between the simulated and actual on/off current ratios. This was due to the experimental device having a lower on current and higher off current than in the simulation. At a thickness of 200 nm, the semiconductor layer was found to be depleted to 85 % of its depth at zero V_{GS}, significantly limiting the on current. The doping level was difficult to predict and was underestimated in the simulation [8]. The higher carrier concentration in the experiment resulted in a shallower depletion region for the same gate voltage as compared to the simulation, limiting the off current. Gate leakage also contributed to a larger off current.

The on/off current ratio should be increased if the OMESFET is to be a practical device. The on current may be boosted by using a thicker and more conductive semiconductor. This might be done by controllably doping rr-P3HT, using a different solvent [3], or using an altogether different material. Since a more conductive semiconductor is more difficult to deplete, an increase in thickness would be constrained by the desired threshold voltage. The off current is currently limited by leakage from the gate. By improving the Schottky junction to reduce its reverse current, the off current of the OMESFET could be reduced.

For the OMESFET to be truly compatible with inexpensive printing methods, the metal layers should be replaced with solution processable materials. This should be possible as all polymer Schottky junctions have been reported [12].

V. CONCLUSIONS

Solution processable polymer semiconductors offer the possibility of inexpensively produced flexible electronic devices. The electrical properties of these materials pose a unique challenge in the development of practical transistors for such an application. Specifically, the operating voltage needed is inconvenient for low power, portable applications. We proposed a solution in the form of an organic metal semiconductor FET (OMESFET) using an aluminum gate and an rr-P3HT channel. Simulations of the device proved the concept as viable and gave a threshold voltage of 5 V and an on/off current ratio of 10^4. The prototype device had a threshold voltage of 3.5 V, a conductance of 6.6×10^{-12} S, a transconductance of 2×10^{-11} S, and an on/off ratio of 24.6. By boosting the OMESFET's on current and reducing its off current, it could be used for digital logic applications.

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